	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments
1	BRS	L1	37572	(fpga pla pld (programmable adj logic adj (array device)))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/15 14:37	
2	BRS	L2	451	1 and ((substrate body well backgate) near3 bias$4)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/15 15:39	
3	BRS	L3	668	1 and (critical adj path)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/15 14:38	
4	BRS	L4	12466	1 and cost	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/15 14:39	
5	BRS	L5	7	2 and 3	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/15 14:39	
6	BRS	L6	232	2 and 4	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/15 15:11	
7	BRS	L8	23	6 and (configuration adj2 data)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/15 15:11	
8	BRS	L9	34	1 and (((substrate body well backgate) near3 bias$4) same configuration)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/15 15:40	